WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor layer formed on a main surface of an insulating layer,

a first transistor forming region formed on a main surface of said semiconductor layer and including a plurality of MOS field effect transistors of a first conductivity type and first field oxide films respectively isolating the plurality of MOS field effect transistors of the first conductivity type;

a second transistor forming region formed on the main surface of said semiconductor layer and including a plurality of MOS field effect transistors of a second conductivity type and second field oxide films respectively isolating the plurality of MOS field effect transistors of the second conductivity type; and

a third field oxide film formed so as to cover the main surface of said semiconductor layer and to reach the main surface of said insulating layer, and isolating said first transistor forming region and said second transistor forming region.

2. The semiconductor device as recited in claim 1, comprising:

a first electrode penetrating through said first field oxide film and electrically connected to said semiconductor layer in said first transistor forming region; and

a second electrode penetrating through said second field oxide film and electrically connected to said semiconductor layer in said second transistor forming region.

3. A semiconductor device, comprising:

a semiconductor layer formed on a main surface of an insulating layer;

a first transistor forming region formed on a main surface of said semiconductor layer and including a plurality of MOS field effect transistors of a first conductivity type and first field shield gate electrodes respectively isolating the plurality of MOS field effect transistors of the first conductivity type;

a second transistor forming region formed on the main surface of said semiconductor layer and including a plurality of MOS field effect transistors of a second conductivity type and second field shield gate electrodes respectively isolating the plurality of MOS field effect transistors of the second conductivity type; and

a field oxide film formed so as to cover the main

surface of said semiconductor layer and to reach the main surface of said insulating layer, and isolating said first transistor forming region and said second transistor forming region.

4. The semiconductor device as recited in claim 3, comprising:

a first electrode electrically connected to said semiconductor layer in said first transistor forming region; and

a second electrode electrically connected to said semiconductor layer in said second transistor forming region.

5. The semiconductor device as recited in claim 3, wherein

said first field shield gate electrode is formed in said first transistor forming region, and a recessed portion is provided in said first transistor forming region positioned at an end portion of said first field shield gate electrode, and

said second field shield gate electrode is formed in said second transistor forming region, and a recessed portion is provided in said second transistor forming region positioned at an end portion of said second field

shield gate electrode.

6. The semiconductor device as recited in claim 3, including

a first impurity region of the second conductivity type formed in said semiconductor layer in an outer region of said first field shield gate electrode and holding said semiconductor layer at a prescribed potential, and

a first impurity region of the first conductivity type formed in said semiconductor layer in an outer region of said second field shield gate electrode and holding said semiconductor layer at a prescribed potential.

7. The semiconductor device as recited in claim 6, wherein

a prescribed groove is provided at an interface between said first impurity region of the first conductivity type and said first impurity region of the second conductivity type.

8. The semiconductor device as recited in claim 6, including

a second impurity region of the first conductivity type lower in an impurity concentration than said first impurity region of the first conductivity type in an outer

region of said first impurity region of the first conductivity type, and

a second impurity region of the second conductivity type lower in an impurity concentration than said first impurity region of the second conductivity type in an outer region of said first impurity region of the second conductivity type.

9. The semiconductor device as recited in claim 3, including

an impurity region of the first conductivity type formed in said semiconductor layer between said first field shield gate electrode and said second field shield gate electrode and holding said semiconductor layer at a prescribed potential.

10. The semiconductor device as recited in claim 3, including

a high concentration impurity region formed in the vicinity of a source region under a gate electrode of said MOS field effect transistor of the second conductivity type and having an impurity concentration higher than said source region.

11. The semiconductor device as recited in claim 4,

wherein

said first electrode is electrically insulated from said first field shield gate electrode, and

said second electrode is electrically isolated from said second field shield gate electrode.

12. The semiconductor device as recited in claim 4, wherein

said first electrode is electrically connected to said first field shield gate electrode, and

said second electrode is electrically connected to said second field shield gate electrode.

13. The semiconductor device as recited in claim 4, wherein

said first electrode is disposed outside a plan region of said first field shield gate electrode, and

said second electrode is disposed outside a plan region of said second field shield gate electrode.

14. The semiconductor device as recited in claim 4, wherein

said first field shield gate electrode includes a main first field shield gate electrode extending in a direction orthogonal to a direction of a gate electrode of

said MOS field effect transistor of the first conductivity type, and two sub first field shield gate electrodes orthogonal to said main first field shield gate electrode, said first electrode being provided between the two sub first field shield gate electrodes, and

said second field shield gate electrode includes a main second field shield gate electrode extending in a direction orthogonal to a direction of a gate electrode of said MOS field effect transistor of the second conductivity type, and two sub second field shield gate electrodes orthogonal to said main second field shield gate electrode, said second electrode being provided between the two sub second field shield gate electrodes.

15. The semiconductor device as recited in claim 4, wherein

said first electrode is connected to said semiconductor layer between two arbitrary gate electrodes of said plurality of MOS field effect transistors of the first conductivity type, and

said second electrode is connected to said semiconductor layer between two arbitrary gate electrodes of said plurality of MOS field effect transistors of the second conductivity type.

16. A semiconductor device, comprising:

a semiconductor layer formed on a main surface of an insulating layer;

a first transistor forming region formed on a main surface of said semiconductor layer and including a plurality of MOS field effect transistors of a first conductivity type and first field shield gate electrodes respectively isolating said plurality of MOS field effect transistors of the first conductivity type;

a second transistor forming region formed on the main surface of said semiconductor layer and including a plurality of MOS field effect transistors of a second conductivity type and second field shield gate electrodes respectively isolating the plurality of MOS field effect transistors of the second conductivity type; and

a mesa isolation region isolating said first transistor forming region and said second transistor forming region.

17. The semiconductor device as recited in claim 16, comprising:

a first electrode electrically connected to said semiconductor layer in said first transistor forming region; and

a second electrode electrically connected to said

semiconductor layer in said second transistor forming region.

18. The semiconductor device as recited in claim 16, including

a third field shield gate electrode formed at an end surface portion of said semiconductor layer of said mesa isolation region.

19. The semiconductor device as recited in claim 16, wherein

said first field shield gate electrode is formed in said first transistor forming region and a recessed portion is provided in said first transistor forming region positioned at an end portion of said first field shield gate electrode, and

said second field shield gate electrode is formed in said second transistor forming region and a recessed portion is provided in said second transistor forming region positioned at an end portion of said second field shield gate electrode.

20. The semiconductor device as recited in claim 16, including

a first impurity region of the second conductivity

type formed in said semiconductor layer in an outer region of said first field shield gate electrode and holding said semiconductor layer at a prescribed potential, and

a first impurity region of the first conductivity type formed in said semiconductor layer in an outer region of said second field shield gate electrode and holding said semiconductor layer at a prescribed potential.

21. The semiconductor device as recited in claim 20, wherein

a prescribed groove is provided at an interface between said first impurity region of the first conductivity type and said first impurity region of the second conductivity type.

22. The semiconductor device as recited in claim 20, including

a second impurity region of the first conductivity type lower in an impurity concentration than said first impurity region of the first conductivity type in an outer region of said first impurity region of the first conductivity type, and

a second impurity region of the second conductivity type lower in an impurity concentration than said first impurity region of the second conductivity type in an

outer region of said first impurity region of the second conductivity type.

23. The semiconductor device as recited in claim 16, including

an impurity region of the first conductivity type formed in said semiconductor layer between said first field shield gate electrode and said second field shield gate electrode and holding said semiconductor layer at a prescribed potential.

24. The semiconductor device as recited in claim 16, including

a high concentration impurity region formed in the vicinity of a source region under a gate electrode of said MOS field effect transistor of the second conductivity type and having an impurity concentration higher than said source region.

25. The semiconductor device as recited in claim 17, wherein

said first electrode is electrically insulated from said first field shield gate electrode, and

said second electrode is electrically isolated from said second field shield gate electrode.

26. The semiconductor device as recited in claim 17, wherein

said first electrode is electrically connected to said first field shield gate electrode, and

said second electrode is electrically connected to said second field shield gate electrode.

27. The semiconductor device as recited in claim 17, wherein

said first electrode is disposed outside a plan region of said first field shield gate electrode, and

said second electrode is disposed outside a plan region of said second field shield gate electrode.

28. The semiconductor device as recited in claim 17, wherein

said first field shield gate electrode includes a main first field shield gate electrode extending in a direction orthogonal to a direction of a gate electrode of said MOS field effect transistor of the first conductivity type, and two sub first field shield gate electrodes orthogonal to said main first field shield gate electrode, said first electrode being provided between the two sub first field shield gate electrodes, and

said second field shield gate electrode includes a main second field shield gate electrode extending in direction orthogonal to a direction of a gate electrode of said MOS field effect transistor of the second conductivity type, and two sub second field shield gate electrodes orthogonal to said main second field shield gate electrode, said second electrode being provided between the two sub second field shield gate electrodes.

29. The semiconductor device as recited in claim 17, wherein

said first electrode is connected to said semiconductor layer between two arbitrary gate electrodes of said plurality of MOS field effect transistors of the first conductivity type, and

said second electrode is connected to said semiconductor layer between two arbitrary gate electrodes of said plurality of MOS field effect transistors of the second conductivity type.

30. A method of manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a substrate;

forming a semiconductor layer on said insulating film;

forming an oxide film on said semiconductor layer and forming at a prescribed position a first field oxide film in plural reaching said insulating film with an LOCOS method; and

forming a second field oxide film smaller in thickness than said first field oxide film again with an LOCOS method in a region sandwiched by said first field oxide films.

31. A method of manufacturing a semiconductor device, comprising the steps of:

forming an insulating film on a substrate;

forming a semiconductor layer on said insulating film;

forming an oxide film on said semiconductor layer and forming a first field oxide film having a first width and a second field oxide film having a second width smaller than said first width with an LOCOS method; and

oxidizing only said first field oxide film and growing said first field oxide film in thickness until said first field oxide film reaches said insulating film again with an LOCOS method.

32. A method of manufacturing a semiconductor device, comprising the steps of:

forming an insulating film on a substrate;

forming a semiconductor layer on said insulating film;

forming an oxide film on said semiconductor layer;

forming a nitride film on said oxide film;

forming on said nitride film a resist film having a prescribed pattern, and etching said semiconductor layer to a prescribed depth with said resist film used as a mask to form a recessed portion of a prescribed depth in said semiconductor layer;

removing said resist film, and then forming again a resist film having a prescribed pattern to pattern the nitride film positioned between said recessed portion and said recessed portion with the resist film used as a mask; and

removing said resist film, and then forming a first field oxide film obtained by growth of an oxide film in said recessed portion reaching the insulating film and a second field oxide film between said recessed portion and said recessed portion with an LOCOS method.

33. A method of manufacturing a semiconductor device, comprising the steps of:

forming an insulating film on a substrate;

forming a semiconductor layer on said insulating

film;

forming an oxide film on said semiconductor layer;

forming a buffer layer on said oxide film;

forming a nitride film on said buffer layer;

forming on said nitride film a first resist film having a first opening portion and a second opening portion wider than said first opening portion and etching said nitride film until a surface of said buffer layer is exposed with said first resist film used as a mask;

forming a second resist film so as to fill only said first opening portion and etching said buffer layer with said first resist film and said second resist film used as a mask; and

removing said first and second resist films, and then forming a first field oxide film reaching said insulating film at a position of said first opening portion and a second field oxide film at a position of said second opening portion with said nitride film used as a mask with an LOCOS method.